Dynamic Configuration of Storage Arrays

ABSTRACT

A reconfigurable memory having M bit lines and a plurality of row lines, where M>1. The memory includes an array of memory storage cells, each memory storage cell storing a data value. The data value is read from or into the storage cells by coupling that data value to one of the bit lines in response to a row control signal on one of the row lines. A row select circuit generates the row control signal on one of the row lines in response to a row address being coupled to the row select circuit. The row select circuit includes a memory for storing a mapping of the row addresses to the row lines that determines which of the row lines is selected for each possible value of the row address. The memory includes a plurality of sense amplifiers, one such sense amplifier being connected to each of the bit lines for measuring a signal value on that bit line. A controller that is part of the memory tests the memory storage cells both at power up and run time to detect defective memory storage cells. The controller uses an error correcting code scheme to detect errors during the actual operation of the memory. The memory includes sufficient spare rows and columns to allow the controller to substitute spares for rows or columns having defective memory storage cells.